



Power-On Self-Test (POST) for the Intel® PXA27x Processor Developer's Kit

Software Release Notes

Release Version 4.05.010.1.1, Beta

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1.0 Description

This package contains version 4.05.010.1.1, Beta, of the Power-On Self-Test (POST) for the Intel® PXA27x Processor Developer's Kit (DVK). This version of POST works with the Intel® PXA27x Processor Developer's Kit Processor Card (processor card) using the Intel® PXA27x processor family (PXA27x processor).

POST is useful as a manufacturing test and as a confidence test for the DVKs. Although this software has had validation testing, it is used as EXAMPLE CODE ONLY and cannot be used "as is" for production systems. No warranty, expressed or implied, is to be associated with this software and the user assumes all risk.

1.1 Kit Contents

This kit includes a self-extracting file, POST_PXA27x_V4_05_010.exe, which contains:

- POST Binary Files
 - The binary version of POST that can be programmed into either the flash memory on the processor card or the flash memory on the DVK's Main Board (main board). There are binary files that support different processor configurations and can be found in the installation directory.
 - POST_PXA270_PXA272_V4_05_010.bin
The POST that is programmed into the processor card or the main board flash and supports the Intel® PXA270 and PXA272 processor configurations (32 bit).
 - POST_PXA271_V4_05_010.bin
The POST that is programmed into the processor card or the main board flash and supports the Intel® PXA271 processor (16 bit).
- POST_PXA27x_V4_05_010.zip
All of the source files that can be modified and then rebuilt into the binaries. These files can be found in the installation directory.
- RelNote_POST_MB.htm
The release notes that describe this release (this file) can be found in the installation directory.
- SWLicense.pdf
A copy of the general software End-User License Agreement (EULA) can be found in the installation directory.

1.2 Related Documentation

Related documentation for this kit includes:

- *Intel® PXA27x Processor Developer's Kit User's Guide* — See the Related Documents section in the Introduction and Startup chapter of this User's Guide for a complete list of all related documentation, including descriptions of all related switches.
- *Diagnostics for the Intel® PXA27x Processor Developer's Kit User's Guide* — Provides a complete description of the POST and BBU programs, and information about setting frequencies.
- *Flash Memory Programmer for Intel® Development Platforms Release Notes* — Provides more details of the JFlashMM software.
- *Intel® XDB JTAG Debugger for Intel® JTAG Cable User's Manual* — Provides information about using the flash programming plug-in for the Intel® XDB JTAG Debugger.



1.3 Software Required

The following software is required:

- For the DVK, JFlashMM V5.01.007 or higher, or the Intel® XDB JTAG Debugger is used to program the flash memory on the processor card. Refer to the [Pointer to JFlashMM Software](#) section for more information.
- One of the terminal emulator programs listed below installed on the PC:
 - HyperTerminal*
 - Tera Term Pro*
- Board Bring Up (BBU) version V1.00.031 for the Intel® PXA270 and PXA272 processors.
- Board Bring Up (BBU) version V1.01.032 for Intel® PXA271 processor.

1.4 Supported Hardware Revisions

1.4.1 DVK Support

This image has been tested with the following DVK specifications:

Table 1: DVK Specifications

Main Board Revision	Main Board ECO Revision	Daughter Card Revision	Daughter Card ECO Revision	Processor Stepping	Power Management Integrated Circuit (PMIC) Board Revision	PMIC ECO Revision
2.1	C	1.2	E	C0	1.2	D

Note: The stepping of the processor can be viewed from the opening screen of POST. The stepping is also reported by the JFlashMM utility on any access to the target system.

2.0 Build Instructions

This version of POST is built using ARM ADS 1.1. The ARM project file named P4MB_XLLP.mcp included in the kit has multiple targets available. Table 2 identifies the target that must be selected to build each of the binaries included in this kit. Each binary file that is created has the same name, but is placed into a subdirectory with the name of the target selection from Table 2.

Table 2: Target Build Selections

Target Selection	Binary File Created
Bootable_Discrete_C0/C5	POST_PXA270_PXA272_V4_05_010.bin
Bootable_Discrete_C0_MCP	POST_PXA271_V4_05_010.bin

3.0 Supported Features for this Release

3.1 New Features for Patch 4.05.010.1.1

The following list indicates the new features implemented in this release:

- POST initial boot up now supports the C5 stepping of the Intel® PXA27x Processor.
- The target selected to build the binary file POST_PXA270_PXA272_V4_05_010.bin now supports the C0/C5 stepping of the Intel® PXA27x Processor.

3.2 Changes for Release 4.05.010

The following list indicates the new features implemented in this release:

- The code has been conditioned to run from the processor card or the main board flash with the optimum memory timings usable for either configuration. The POST runs with the highest performance when programmed onto the processor card flash.
- Modifications to the memory controller settings for PCMCIA devices have been made to support the highest frequency settings.
- Updates the version of XLLP to V1.01.034.

4.0 Known Problems

- IrDA test fails on the first attempt to run but then passes on subsequent runs.
- USIMs test does not work.
- DVM test is no longer valid for this hardware configuration and will hang the system.
- The POST application incorrectly identifies the C5 stepping of the Intel® PXA27x Processor as a C4 stepping.

5.0 Hardware Required

- DB-9 null-modem serial cable (included with kit)
- Low power Ethernet card* (from Socket Communications, Inc.) in a PCMCIA adapter
- MMC Card or SD Card (included with the kit) is supported. The IrDA probe from ACTiSYS ACT-IR220LN (recommended) or a similar probe with 115200 baud. The Extended Systems* ESI-09680-7501 probe is a similar probe.
- Memory Stick*
- Headphones – Any standard headphones
- Intel® JTAG Cable assembly with “rev 4” label attached (included with kit)

Note: All applicable ECOs must be applied for the software to operate properly.

6.0 Procedure

The following procedures assume that the CPLD and FPGA have been pre-programmed on the DVKs.

There are two banks of flash memory on the DVKs. One bank is on the processor card and the other is on the main board.

Note: The flash on the main board contains a factory installed version of POST and BBU. The standard JFlashMM software is used for programming the flash memory. It is recommended that the POST software is installed on the flash memory of the processor card.

Note: The DVKs have a BBU and POST co-resident in flash memory. The BBU and the POST program can be executed through commands or by switch settings shown in the [Factory Default Switches and Setup for the DVKs](#) section.

6.1 Setting Up the Testing Environment

To program the flash memory with a POST image, use JFlashMM software or the Intel® XDB JTAG Debugger for Intel® JTAG Cable as discussed in the following sections. The terminal emulator must also be setup.

6.1.1 Flash Programming Software

Two applications can be used for programming the flash memory with a POST image. The easiest method is to use JFlashMM software. Another method, which has a speed advantage, is to use the Intel® XDB JTAG Debugger for Intel® JTAG Cable.

6.1.1.1 Pointer to JFlashMM Software

For more information on JFlashMM software refer to the *Flash Memory Programmer for Intel® Development Platforms Release Notes*. Run the downloaded software to install the JFlashMM software on the PC.

6.1.1.2 Pointer to Intel® XDB JTAG Debugger

The Intel® XDB JTAG Debugger can be used for programming the flash memory. Contact the application engineer or local service organization for information about how to obtain this software and related documentation.

6.1.2 Setting Up the Terminal Emulator

Connect the DB-9 Serial connection to the FFUART (J2) on the daughter card. This is the primary I/O for POST software. A terminal emulator such as HyperTerminal* or Tera Term Pro* is the primary I/O device for POST. Create a terminal setup as shown in Table 3.

Table 3: Terminal Setup Settings

Setting	Value
Baud Rate	115,200 baud
Data Bits	8
Parity	None
Stop Bits	1
Flow Control	None



6.2 Factory Default Switches and Setup for the DVKs

Refer to the following sections to select the appropriate switch settings for the DVKs.

6.2.1 Switch Setup

Set the discrete switches to the settings indicated in Table 4. The factory default settings below are required for a standard execution of POST, which runs with the core clock at 520 MHz for the Intel® PXA27x Processor. Table 4 describes the switches relevant to POST. The BBU may use these switches differently.



Table 4: Switch Description

Switch ID	Description	Default Settings	Action
SW5	IrDA	DOT	Connects the IrDA circuitry to the controller.
SW7	SWAP Flash	DOT	DOT = Processor Card Flash NO DOT = Main Board Flash
SW8	Flash Width Select	DOT	Must be set to the DOT position.
SW9	FPGA_RESET	DOT	Run
SW10	NBATT_Fault	DOT	Normal
SW11	nVDD_Fault	DOT	Normal
SW12	Operating Frequency for POST (default is 520 MHz)	A	See the Setting Frequencies chapter in the <i>Intel Diagnostics for Intel® PXA27x Processor Developer's Kit Architecture User's Guide</i> for more information.
SW13	Operating Frequency for POST (default is 520 MHz)	D	See the Setting Frequencies chapter in the <i>Intel Diagnostics for Intel® PXA27x Processor Developer's Kit User's Guide</i> for more information.
SW14	Fast Bus Select	NO DOT	DOT = normal system bus operation NO DOT = Fast (System) Bus operation
SW15	SDCLK Select	DOT	DOT = MCik/2 NO DOT = MCik
SW16	Turbo Mode	NO DOT	DOT = Turbo mode off NO DOT = Turbo mode on
SW17	Alternate Boot	DOT	DOT = Boot POST NO DOT = Boot BBU
SW18	Alternate I/O	DOT	DOT = FFUART for I/O NO DOT = BTUART for I/O NOTE: If no serial cable is detected on the FFUART when set to DOT, and SW20 and SW21 are set to DOT, the POST will redirect the serial data to the LCD and loop the Normal Suite of tests. NOTE: A terminal emulator must be active on the host machine for the serial cable to be detected by the POST.
SW19	Alternate Error Handler	DOT	DOT = Normal mode NO DOT = Debug Mode or Virtual Switch Mode. NOTE: Virtual Switch Mode requires an external software program that has not been released yet. The POST has the capability to use this tool when it is available.
SW20	POST RUN MODE SELECT BIT 0	DOT	See Table 5 for the POST Run Modes.
SW21	POST RUN MODE SELECT BIT 1	DOT	See Table 5 for the POST Run Modes.

Table 5 shows how to select the POST Run Modes. There are three different test suites and a command mode that is selectable.

Table 5: POST Run Modes

SW21	SW20	Run Mode
DOT	DOT	Normal – POST runs all non-interactive tests.
DOT	NO DOT	Interactive – POST runs all non-interactive and interactive tests that can be run with components that come with the DVKs, such as the MMC card.
NO DOT	DOT	Manufacturing – POST runs all non-interactive and interactive tests for all tested components. This may require hardware that does not ship with the DVKs such as a USIM card.
NO DOT	NO DOT	Command – POST does not run any tests, but rather presents a prompt to receive commands from the user via the terminal emulator. This is also called "String Mode".

Table 6 identifies the default settings for each of the switches in SW1 on the daughter card.

Table 6: Daughter Card SW1 Positions

Switch – Position	Default setting	Description
SW1-8	On	On = Intel® PXA27x processor clock is from PXTAL (Crystal or OSC). Off = Intel® PXA27x processor clock is from CLK_PIO.
SW1-7	Off	On = Communications processor internal boot. Off = Communications processor external boot.
SW1-6	On	On = 32-bit mode (used for Intel® PXA270 and Intel® PXA272 Processors). Off = 16-bit mode (used for Intel® PXA271 Processor).
SW1-5	On	On = Flash Memory Bank Off = Image Memory Bank
SW1-4	Off	On = Communications processor MSL Baseband is connected. Off = Communications processor MSL Baseband is not connected.
SW1-3	On	General purpose switch for CPLD configuration
SW1-2	Off	On = Connect Communications Processor nCS1 to SRAM1 and SRAM2. Off = Connect Communications Processor nCS1 to SRAM1 and nCS2 to SRAM2.
SW1-1	On	On = JTAG chain connections are determined by JTAG_SEL (SW2). Off = JTAG chain is connected to CPLD1.

Table 7 identifies the default settings for each of the switches in SW2 (JTAG_SEL) on the daughter card:

Table 7: Daughter Card SW2 Positions

SW2-1	SW2-2	Description
On (default)	On (default)	JTAG chain is connected to the Intel® PXA27x processor.
On	Off	JTAG chain is connected to the communications processor.
Off	On	JTAG chain is connected to Intel® PXA27x processor and the communications processor.
Off	Off	JTAG chain is connected to the Intel® PXA27x processor, communications processor, CPLD2, EEPROM, and the FPGA.

6.2.2 Flash Programming Setup

Two images must be programmed into the flash memory on the processor card. The BBU is programmed at address 0, and the POST is programmed at address 0x40000.

6.2.2.1 Intel® XDB JTAG Debugger for Intel® Cable

Connect the Intel® JTAG Cable assembly from the PC parallel port to the JTAG TAP (J4) on the daughter card. Refer to the *Intel® XDB JTAG Debugger for Intel® Cable User's Manual* for information on using the flash programming plug-in.

6.2.2.2 JFlashMM for the DVK

To program flash memory, connect the Intel® JTAG Cable assembly from the PC parallel port to the JTAG TAP (J4) on the daughter card. Refer to the *Flash Memory Programmer for Intel® Development Platforms Release Notes* for information on using JFlashMM.

- The BBU binary is programmed at the default location of address 0. JFlashMM defaults to address 0 and does not require a parameter for this address.
- The POST binary is programmed at address 0x40000.
- Use the following commands to program flash memory at a different base address:
JFlashmm bulbcx POST_PXA270_PXA272_V4_05_010.bin P 40000

6.2.3 Running the POST Program

POST executes on the DVKs upon power up, and messages appear on the terminal emulator application. The HEX LEDs on the main board changes values as POST executes. A test image is displayed on the LCD screen. Follow all instructions given on the terminal window.

Note: Upon completion of POST, the software asserts “STRING MODE” so that commands can be issued to POST.

6.2.4 Detailed Instructions for Selected Tests

This section describes tests that may require some additional hardware or guidelines in order to be completed, for one of the following reasons:

- Setting up or running the test or the user interface may not be intuitive. This may make the test difficult to execute.
- Some hardware components may have problems.
- Some optional hardware has been installed on the development system.

Note: The following list of tests may or may not be required to qualify the hardware integrity of the board. The tests for optional hardware should be executed only if the optional hardware has been installed on the development system.

6.2.4.1 DVM Test

This test is no longer valid for this hardware configuration and will halt the system.

6.2.4.2 Ethernet External Loopback Test

The Ethernet external loopback test requires that a loopback cable assembly be connected to the Ethernet connector. This assembly is an RJ45 connector, and the following pins must be connected:

- Pin 1 (TX+) connected to pin 3 (RX+)
- Pin 2 (TX-) connected to pin 6 (RX-)

6.2.4.3 PCMCIA Tests

For the PCMCIA tests, the slot numbers are: 0 at Top and 1 at Bottom.

6.2.4.4 HEX Switch Test

This test requires rotating the switches one complete turn. If the switches are turned too quickly, an error can occur. Turn the switches at a rate that allows the HEX display to be viewed. The rightmost digit in the HEX display is used to show the setting of the switch.

6.2.4.5 Intel® Mobile Scalable Link Loopback Test (Optional)

The Intel® Mobile Scalable Link (Intel® MSL) loopback test requires that the Intel® MSL loopback assembly be attached to the Intel® MSL header J15. Attach the gray cable from the connector on the assembly that is the END connector. The END connector is the only connector that is oriented 90° from the other two connectors.

Issue the command:

```
MSL.MFGLOOPBACK
```

Note: This test requires a cable that is not provided with the DVK.

6.2.4.6 Fastap* Keypad Tests

The Fastap* keypad test command is:

```
FASTAP
```

6.2.4.7 Infrared Tests

The IrDA probe from ACTiSYS ACT-IR220LN is recommended for use with this test.

6.2.4.8 Camera Test

The camera test is currently executed from the BBU code. Perform this test as follows:

1. Set the SW12 and SW13 Hex switches to AD.
2. Leave switches SW14 and SW16 in the NO DOT position; set switch SW15 to the DOT position.
3. Prepare to boot BBU by setting SW17 to the NO DOT position.
4. Power cycle the board. This will present the BBU startup screen.
5. At the BBU prompt, type the commands as listed in Table 8.

Table 8: BBU Command Descriptions

Step	Command	Description
a.	MPTS	Moves the program to SRAM.
b.	LBKL 0xFF	Sets the LCD backlight to full intensity.
c.	ILCD	Initializes the LCD controller.
d.	LCDB	Sets the LCD screen to blue (optional step).
e.	ICAM	Initializes the camera and the camera controller.
f.	CAMV 0x20	Camera video mode – gets 32 frames of video (as specified by hex number entered).

6. After executing the CAMV command, the LCD screen will show a rough image of the camera image. This image will update for about 15 seconds and then stop, which means that the test has passed.

6.2.4.9 USIM Tests

There are two brands of USIM cards that are in use at this time. The POST requires slightly different behavior for the different brands. There are Rohde & Schwarz and Schlumberger models. The Rohde & Schwarz brand has some blue coloring on the surface and the Schlumberger brand is pure white. The USIM test must be executed through the command interface and depends on the brand of the USIM card.

The white (Schlumberger) is tested with the command:

USIMW

The blue (Rohde & Schwarz) is tested with the command:

USIMB

Note: This test is not functional in this release.

6.2.4.10 USBOTG Transceiver Test

The USBOTG transceiver is multiplexed with the FFUART circuitry; therefore the test is executed with the terminal emulator connected to the BTUART. Set SW18, SW20, and SW21 into the NO DOT position. This sets the POST into Command Mode and initializes the BTUART as the primary I/O.

Reboot the system, and when the command prompt is presented, type the command:

USBOTG.DUMPREG

Follow the instructions on the screen to complete the test.

6.2.4.11 USB Enumeration Test

Run this test manually by typing the command:

```
USB.ENUMERATE, 1
```

6.2.5 Programming the Unique MAC Address

All DVKs have had their unique MAC address pre-set at the factory.

Upon completion of POST, program the MAC address.

1. From the string mode, issue a POST command to address the Ethernet card. For example:

```
ETHERNET.SETMACADDRESS, 0F3344667788<CR>
```

Use the appropriate MAC address for this environment.

2. POST programs the MAC address into the EEPROM and respond with the following messages:

```
LAN91C111 User supplied MAC Address: 0F-33-44-66-77-88
```

```
LAN91C111 EEPROM MAC Address: 0F-33-44-66-77-88
```

3. The MAC address stored in the EEPROM can be verified by issuing the following command:

```
ETHERNET.GETMACADDRESS<CR>
```

4. POST reads the MAC address stored in the EEPROM and responds with the message:

```
LAN91C111 EEPROM MAC Address: 0F-33-44-66-77-88
```